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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/888,521	06/26/2001	Andrew M. Volk	2207/11504	1112

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EXAMINER	
BUTLER, DENNIS	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/888,521	VOLK, ANDREW M.	
	Examiner	Art Unit	
	Dennis M. Butler	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This action is in response to the application filed on June 26, 2001. Claims 1-30 are pending.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 12-16 and 18-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Kopser et al., U. S. Patent 6,629,250.

Per claims 12,18, 20, 22, 24 and 26:

A) Kopser et al teach the following claimed items:

1. connecting a first interface/agent (circuit #1) to a second interface/receiver/agent (circuit #2) with interconnect comprising traces having varying lengths with figure 1 and at column 3, lines 1-9;

2. generating and outputting a multi-bit data signal to the traces at column 3, lines 10-30 and at column 6, line 66 – column 7, line 12;

3. a plurality of programmable delay outputs, each provided on a terminal end of one of the traces (receiver end) and providing a delay corresponding to a difference between the length of the respective trace and the length of a longest trace with figure 2, at column 2, lines 15-24 and 38-43, at column 4, lines 5-18 and at column 6, line 66 – column 7, line 12.

Per claims 13-16, 19, 21, 23, 25 and 27-29:

Kopser describes a plurality of variable delay outputs from the delay element, selecting one of the plurality in accordance with a length of a trace and programming the delay by software with variable delay circuit 26 and select register 34 of figure 2, at column 4, lines 5-40. Kopser describes that the delay is inversely proportional to the lengths (the longest trace has the least delay and the shortest trace has the most delay) and the delay is proportional to a difference between the respective lengths and the length of a longest trace (the

longest trace has the least delay and the shortest trace has the most delay) at column 6, line 66 – column 7, line 12. Kopser describes no delay output is provided for the longest trace at column 7, lines 1-5. Kopser describes the terminal end is at a receiver interface with circuit #2 of figure 1 and at column 6, line 66 – column 7, line 12. Kopser describes the delay element comprises a plurality of multiplexers each coupled between a buffer (master latch 20) and a plurality of variable delay outputs (outputs of delay elements 32) with multiplexers 32 of figure 2, at column 2, lines 38-43 and at column 6, line 66 – column 7, line 12. Kopser describes a plurality of programmable registers to select one of the plurality of variable delay outputs in accordance with a length of a trace with select registers 34 of figure 2, at column 2, lines 38-43, at column 4, lines 35-37 and at column 6, line 66 – column 7, line 12.

6. Claims 1-11, 17 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kopser et al., U. S. Patent 6,629,250 in view of Schoenfeld et al., U. S. published application 2002/0091958.

Per claim 1:

A) Kopser et al teach the following claimed items:

1. a driver interface with sending circuit 10 of figure 1;

2. a receiver interface coupled to the driver via an inter connect comprising a plurality of varying length traces with receiving circuit 12 and the transmission lines of figure 1 and at column 3, lines 1-9;

3. a programmable delay element programmed by a delay corresponding to a length of a trace traveled by a respective signal with variable delay circuit 26 and select register 34 of figure 2, at column 2, lines 38-43, at column 4, lines 35-37 and at column 6, line 66 – column 7, line 12.

B) The claims seem to differ from Kopser in that Kopser fails to explicitly teach the programmable delay element coupled to the driver interface to delay switching of output signals of the driver interface as claimed.

C) However, Kopser describes providing the delay element at the receiver interface for adding the recited delay to the received data signals at column 6, line 66 – column 7, line 12. Schoenfeld teaches that it is known to provide a programmable delay element (delay 138) coupled to the driver interface (output buffer 140) to delay switching of output signals of the driver interface with figure 2 and at page 4, paragraphs 30 and 32 . It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a programmable delay element (delay 138) coupled to the driver interface (output buffer 140) to delay switching of output signals of the driver interface, as taught by Schoenfeld, in order to reduce the spread in time of the data output signals for allowing more reliable and stable data sampling at the receiver interface. One of ordinary skill in the art would have been motivated to combine Kopser and Schoenfeld because of Schoenfeld's suggestion that providing programmable delay elements at the output lines would decrease output skew of the data output signals at paragraphs 7 and 11. It would have been obvious for one of ordinary

skill in the art to combine Kopser and Schoenfeld because they are both directed to the problem of aligning a plurality of data signals transmitted on a data bus having a plurality of traces in order to reliably sample the plurality of data signals with a single clock signal.

Per claims 2-8:

Kopser describes that the delay is inversely proportional to the lengths (the longest trace has the least delay and the shortest trace has the most delay) and the delay is proportional to a difference between the respective lengths and the length of a longest trace (the longest trace has the least delay and the shortest trace has the most delay) at column 6, line 66 – column 7, line 12. Kopser describes a plurality of variable delay outputs from the delay element, selecting one of the plurality in accordance with a length of a trace and programming the delay by software with variable delay circuit 26 and select register 34 of figure 2, at column 4, lines 5-40. Kopser describes no delay output is provided for the longest trace at column 7, lines 1-5. Schoenfeld describes providing his driver interface to a DDR SDRAM device at paragraph 9. It would be obvious to apply Schoenfeld's driver interface to a memory controller. Claims 4 and 8 recite obvious variations of well-known interface and timing element and would have been obvious in view of the teachings of Kopser and Schoenfeld.

Per claim 9:

A) Kopser et al teach the following claimed items:

1. a plurality of output latches of a first interface are inherently included in sending circuit 10 of figure 1 in order to synchronously transmit data to receiving circuit 12 as shown with figure 1 and at column 3, lines 57-62;

2. interconnect coupling the output latches to a second interface (receiving circuit 12) comprising a plurality of traces of varying length that propagate signals from the output latches to the second interface with receiving circuit 12 and the transmission lines of figure 1 and at column 3, lines 1-9;

3. a plurality of multiplexers with multiplexers 32 of figure 2, at column 2, lines 38-43 and at column 6, line 66 – column 7, line 12;

4. a plurality of programmable registers to select one of the plurality of variable delay outputs in accordance with a length of a trace with select registers 34 of figure 2, at column 2, lines 38-43, at column 4, lines 35-37 and at column 6, line 66 – column 7, line 12.

B) The claims seem to differ from Kopser in that Kopser fails to explicitly teach that each multiplexer is coupled between a latch of the output latches and a delay element comprising a plurality of variable delay outputs as claimed.

C) However, Kopser describes that each multiplexer is coupled to a plurality of variable delay outputs with variable delay circuit 26, multiplexer 30 and select register 34 of figure 2, at column 4, lines 5-40. Kopser describes that multiplexer 30 is located in receiving circuit 12. Therefore, multiplexer 30 is electrically coupled to the output latches through master latch 20. Kopser does not describe that multiplexer 30 is located between the output latch and the delay. However,

multiplexer 30 is coupled to both elements. Each multiplexer includes a programmable register that is programmed to select a delay in accordance with a length of a trace that propagates a signal of the corresponding latch. Therefore, although multiplexer is placed in a different location than the claimed invention, it achieves the same result and the recited placement of the claimed multiplexer is not critical to achieving the result of selecting the variable delay output in accordance with a length of a trace that propagates the signal from the corresponding output latch. In addition, it would have been obvious to one having ordinary skill in the art at the time the invention was made to locate multiplexer 30 between the output latch and the delay in order to meet space and lay out requirements when designing the actual chip or circuit board. It would have been obvious to one having ordinary skill in the art at the time the invention was made that elements shown on a circuit diagram may be laid out differently when the actual chip or circuit board is constructed.

Per claims 10 and 11:

Kopser describes phase-shifted versions of a clock with the phase shifted clocks input to multiplexer 30 of figure 2. Schoenfeld describes providing his driver interface to a DDR SDRAM device at paragraph 9. It would be obvious to apply Schoenfeld's driver interface to a memory controller coupled to a memory.

Per claims 17 and 30:

Kopser describes loading the software codes into the select registers when power is first applied to the circuits at column 4, lines 35-41. It is well known that

BIOS program routines initialize hardware devices in a computer system when power is first applied. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to program the select registers using a BIOS program when power is first applied in order to initialize the interconnect system.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis M. Butler whose telephone number is 703-305-9663. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dennis M. Butler

Dennis M. Butler

Primary Examiner

Art Unit 2115